REMARKS

Independent Claims 41 and 67 have been amended to expressly recite the interrupt capability of the control unit. Dependent Claims 83 - 86 have been added to claim the invention with more particularity. Accordingly, Claims 41 - 86 are now pending.

Turning to the 27 April 2005 final Office Action and the 14 July 2005 Advisory Action, the Examiner stated on page 2 of the 27 April 2005 Office Action that "The amendment filed 12/10/03, 12/23/03 and 2/11/04 are objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure". By the "amendment filed 12/10/03, 12/23/03 and 2/11/04", Applicants' Attorney once again assumes that the Examiner meant (a) the Amendment submitted 10 December 2003, (b) the Supplemental Amendment submitted 23 December 2003, and (c) the Amendment submitted 11 February 2004 for revising the text, and does not include the further Amendment submitted 11 February 2004 for revising the drawings since the 11 February 2004 Amendment to Drawings does not present any revision(s) to the specification. Subject to this assumption, the objection to the 10 December 2003 Amendment, the 23 December 2003 Supplemental Amendment, and the 11 February 2004 Amendment to Text as introducing new matter into the disclosure is again respectfully traversed.

On page 2 of the 27 April 2005 Office Action, the Examiner again alleged that deletion of the material "which is typically a first in first or (FIFO) buffer" at lines 4 and 5 on page 7 of the specification introduces new matter into the disclosure. Presumably the Examiner again meant the last clause of the sentence "SD 26 demultiplexes and depacketizes the data stream, storing the demultiplexed compressed audio and video data in data buffer 48, which is typically a First-In-First-Out (FIFO) buffer" in the paragraph bridging pages 6 and 7 of the specification.

On page 2 of the Response submitted 1 July 2005, Applicants' Attorney again explained why data buffer 48 cannot actually be a FIFO buffer (in hardware) despite the disclosure in the specification that "SD 26 demultiplexes and depacketizes the data stream, storing the demultiplexed compressed audio and video data in data buffer 48, which is typically a First-In-First-Out (FIFO) buffer". Instead of repeating the prior explanation, the Examiner is simply referred to page 2 of the 1 July 2005 Response and the earlier material referred to there.

On page 3 of the 1 July 2005 Response, Applicants' Attorney pointed to the holding of Ex parte Brodbeck (PTOBA 1977) 199 USPQ 230 that correcting a technical error in a utility U.S. patent application does not introduce new matter if a person skilled in the relevant art would appreciate not only the existence of the error but what the error is. Skilled-artisan affidavit evidence was utilized in Brodbeck to explain why the language at issue was erroneous and how it should be corrected in light of the knowledge of a person skilled in the art.

A declaration of Alin Theodor Iacob, a person of high skill in the semiconductor memory art, accompanied the 1 July 2005 Response to show that persons skilled in the art would recognize that buffer 48 in the specification of the present application is not actually a FIFO or a FIFO buffer. The procedure employed in Brodbeck to correct an error in a U.S. patent application has thus been followed in the present application. In accordance with Brodbeck and In re Oda et al. (CCPA 1971) 170 USPQ 268 cited as authority in Brodbeck, deletion of the material "which is typically a first in first or (FIFO) buffer" at lines 4 and 5 on page 7 of the specification corrects an error that would be readily recognized by persons skilled in the relevant art and does not introduce new matter into the specification.

In regard to the Iacob declaration, the Examiner states on page 2 of the 14 July 2005 Advisory Action that "In reply, please see the final office action Para 6". Paragraph 6, page 6, of the 27 April 2005 Office action states that deletion of the material "which is typically a first in first or (FIFO) buffer" at lines 4 and 5 on page 7 of the specification "is a new matter because the applicant defined the buffer which is a FIFO buffer" and that "The applicant can not delete it in order to modify the scope of the specification". This, however, is not the law for the present situation.

Repeating what was stated above, a technical error in a U.S. patent application can, in accordance with Brodbeck and Oda, be corrected by presenting skilled-artisan evidence to show why the technical language is incorrect and how it should be corrected in light of the knowledge of a person skilled in the art. Since such a showing has been made in the present application, the objection to deletion of the material "which is typically a first in first or (FIFO) buffer" at lines 4 and 5 on page 7 of the specification as introducing new matter into the disclosure of the invention has been overcome.

The Examiner has further alleged on page 2 of the 27 April 2005 Office Action that substitution of the term "buffer" for "FIFO" at page 7, line 7, page 10, lines 12, 26, and 27, page 11, line 30, and page 23, lines 29 and 30, introduces new matter into the disclosure. These changes involve item 48. That is, "FIFO 48" has been changed to "buffer 48" at the foregoing places in the specification.

For the reasons presented on page 5 of the 1 July 2005 Response, changing "FIFO" to "buffer" at the indicated places in the specification completes the correction of an error that would be readily recognized by persons skilled in the relevant art and does not introduce new matter into the specification. As with the first-mentioned new-matter objection, submission of the Iacob declaration overcomes this objection

The net result is that none of the objected-to material introduces new matter into the disclosure. The 35 USC 132 objection to the 10 December 2003 Amendment, the 23 December 2003 Supplemental Amendment, and the 11 February 2004 Amendment to Text as introducing new matter into the specification should now be withdrawn.

Claims 41 - 52, 55 - 60, 62 - 75, and 78 - 82 have again been rejected under 35 USC 103(a) as obvious based on Okada et al. ("Okada"), U.S. Patent 5,668,601, in view of Maturi et al. ("Maturi"), U.S. Patent 5,559,999. This rejection is respectfully traversed in view of the revisions made to independent Claims 41 and 67.

The pertinent material of Okada was summarized in the 10 December 2003 Amendment and repeated on pages 5 and 6 of the 1 July 2005 Response. That material is repeated below for the Examiner's convenience:

> Okada discloses an audio/video decoding system having parser 4, audio decoder 2, and video decoder 3. Parser 4, including internal demultiplexer 5, separates (demultiplexes and depacketizes) an incoming audio/video data stream into an audio data stream, an audio presentation time stamp, a video data stream, a video presentation time stamp, and a system clock reference. The audio presentation time stamp and the audio data stream are respectively sequentially stored in first-in-first-out ("FIFO") register 11 and FIFO bit buffer 12, both of which are components of audio decoder 2. The video presentation time stamp and the video data stream are respectively sequentially stored in FIFO register 21 and FIFO bit buffer 22, both of which are components of video decoder 3. The system clock reference goes to controllers 14 and 24 of respective decoders 2 and 3.
>
> Bit buffers 12 and 22 automatically sequentially provide the audio and video data streams respectively to decoder core circuits 13 and 23 of decoders

2 and 3 for decoding and presentation in synchronism at times determined respectively by controllers 14 and 24. Audio controller 14 determines when audio decode core circuit 13 decodes the current audio data of the audio data stream as a function of the system clock reference, the audio presentation time stamp, and the various transmission-delay/processing times in audio decoder 2. Video controller 24 similarly determines when video decode core circuit 23 decodes the current video data of the video data stream as a function of the system clock reference, the video presentation time stamp, and the various transmission-delay/processing times in video decoder 3. The decoding and presentation of the video data is synchronized to the decoding and presentation of the audio data by way of the system clock reference supplied to controllers 14 and 24.

Applicants' Attorney further noted on page 6 of the 1 July 2005 Response that:

> The foregoing summary applies to a first embodiment of Okada's decoding system as shown in Fig. 1. Audio decoder 32 replaces audio decoder 2 in a second embodiment of Okada's decoding system as depicted in Fig. 2. Audio decoder 32 consists of the components of audio decoder 2 plus time stamp generator 41. In the second embodiment, video decoder 3 becomes video decoder 33 in which video controller 42 replaces video controller 24. A third embodiment of Okada's decoding system, as shown in Fig. 6, also contains audio decoder 32. In the third embodiment, video decoder 33 becomes video decoder 82 in which video controller 83 replaces video controller 42.

The pertinent material of Maturi was similarly summarized in the 10 December 2003 Amendment and repeated on page 6 of the 27 July 2005 Response. The summary of Maturi is likewise repeated below for the Examiner's convenience:

> Maturi discloses an interrupt-based system for decoding an incoming audio/video data stream. Pre-parser 22 parses (demultiplexes and depacketizes) the audio/video data stream, stores the audio and video headers respectively in audio and video buffers 20c and 20a, and stores the audio and video data respectively in audio and video channel buffers 20d and 20b. In storing the audio and video headers in header buffers 20c and 20a, pre-parser 22 interrupts host microcontroller 18 and provides the audio and video headers with respective tags that identify the starting channel-buffer addresses of the audio and video data. In response to the interrupt, microcontroller 18 extracts the presentation time stamps from pre-parser 22 and stores the presentation time stamps in memory 18a. Audio and video decoders 28 and 26 later respectively decode the audio and video data under the synchronism control of microcontroller 18.

Independent Claims 41 and 67, as amended, respectively recite:

41. A decoder system comprising:

a control unit capable of performing multiple tasks and capable of being interrupted during at least one of the tasks to perform at least one other of the tasks;

a data buffer comprising a video input buffer and an audio input buffer;

a stream demultiplexer for receiving an incoming data stream comprising data packets each comprising at least one of (i) encoded video data and a video header that contains video timing information for the encoded video data and (ii) encoded audio data and an audio header that contains audio timing information for the encoded audio data, the stream demultiplexer operating

(a) to demultiplex and depacketize the data packets without interrupting the control unit,

(b) to send the encoded video data to the video input buffer for storage there without the video timing information,

(c) to provide, for use by the control unit, video messages which identify where the encoded video data is stored in the video input buffer and which also deal with the video timing information, and

(d) to send the encoded audio data to the audio input buffer for storage there;

a video decoder that decodes the encoded video data to produce decoded video data utilizing video instructions provided from the control unit as to where the encoded video data is stored in the video input buffer; and

an audio decoder that decodes the encoded audio data to produce decoded audio data.

67. A method comprising:

receiving an incoming data stream comprising data packets each comprising at least one of (i) encoded video data and a video header that contains video timing information for the encoded video data and (ii) encoded audio data and an audio header that contains audio timing information for the encoded audio data;

demultiplexing and depacketizing the data packs without interrupting a control unit capable of performing multiple tasks and capable of being interrupted during at least one of the tasks to perform at least one other of the tasks;

storing the encoded video data in a video input buffer without the video timing information;

providing, for use by the control unit, video messages which identify where the encoded video data is stored in the video input buffer and which also deal with the video timing information;

decoding the encoded video data to produce decoded video data using video instructions provided from the control unit as to where the encoded video data is stored in the video input buffer;

storing the encoded audio data in an audio input buffer; and

decoding the encoded audio data to produce decoded audio data.

Claims 41 and 67 are patentable over Okada and Maturi for the reasons presented on pages 8 - 12 of the 1 July 2005 Response.

In addition, Claims 41 and 67 each now require that the control unit be "capable of performing multiple tasks" and be "capable of being interrupted during at least one of the tasks to perform at least one other of the tasks".

As pointed out on page 12 of the 1 July 2005 Response,

> Furthermore, audio controller 14 and video controller 24 (or 42 or 83) in Okada appear to be rather rudimentary devices. Audio controller 14 appears to be substantially dedicated to controlling audio decode core circuit 13. Nothing in Okada discloses or in any way suggests that audio controller 14 is capable of undergoing interruption to service a component other than audio decode core circuit 13. Video controller 24 (or 42 or 83) similarly appears to be substantially dedicated to controlling video decode circuit 23. Nothing in Okada discloses or in any way suggests that video controller 24 (or 42 or 83) is capable of undergoing interruption to service a component other than video decode core circuit 23.

More particularly, Okada states in col. 6 that:

> The audio controller first computes an audio decoding time based on a delay time inherent to the audio stream processor during decoding operations, and second, computes the timing for audio output based on the computed audio decoding time, the SCR and the audio time stamp. The audio controller controls the output of audio from the audio processing circuit in accordance with the computed output timing.

Okada similarly states later in col. 6 that:

> The video decoder includes a video controller, which first, computes a video decoding time based on an internal delay time of the video stream processor in a decoding operation, and second, computes the timing for a video output based on the computed video decoding time, the SCR and the video time stamp. The video controller controls the output of video from the video stream processor in accordance with the timing of the video output.

Nothing in the preceding portions of Okada discloses or suggests that Okada's audio or video controller has the capability of being interrupted during the performance of one task in order to perform another task.

Nor does anything else in Okada disclose or suggest that its audio or video controller is capable of being interrupted during the performance of one task in order to perform another task. Since each of Claims 41 and 67 now requires that the control unit be "capable of being interrupted during at least one of the tasks to perform at least one other of the tasks", combining Okada and Maturi in the proposed would not achieve the subject matter of Claim 41 or 67 even if there were some motivation or incentive for combining the two references. This is true regardless of whether the Examiner's references to Okada's "controller" or "control unit" means audio controller 14, video controller 24 (or 42 or 83), or both audio controller 14 and video controller 24 (or 42 or 83). Accordingly, Claims 41 and 67 are patentable over Okada and Maturi.

Claims 42 - 52, 55 - 60, and 62 - 66 all depend from (directly or indirectly) from Claim 41. The same applies to new Claims 83 and 84. Claims 68 - 75 and 78 - 82, along with new Claims 85 and 86, all depend (directly or indirectly) from Claim 67. Hence, Claims 42 - 52, 55 - 60, 62 - 66, 68 - 75, and 78 - 86 are patentable over Okada and Maturi for the same reasons as Claims 41 and 67.

Dependent structure Claim 42 recites that "the control unit is interrupted in response to a synchronization signal for reading the video messages provided by the system demultiplexer and for providing the video instructions to the video decoder". Dependent structure Claim 59 similarly recites that, "in response to a synchronization signal generated by the video output processor, the control unit is interrupted for reading the video messages provided by the stream demultiplexer and for providing the video instructions to the video decoder".

Dependent method Claim 68 recites that the method further includes "generating a synchronization signal" and "interrupting the control unit in response to the synchronization signal for causing the control unit to read the video messages and to generate the video instructions". Dependent method Claim 79 similarly recites that the method further includes "utilizing a video output processor that processes the decoded video data to generate a

synchronization signal" and "interrupting the control unit in response to the synchronization signal for reading the video messages and for generating the video instructions".

Inasmuch as neither Okada's audio or video controller is capable of being interrupted during the performance of one task in order to perform another task, Okada does not meet the synchronization-signal requirement of Claim 42, 59, 68, or 79. A separate basis is thereby provided for allowing Claims 42, 59, 68, and 79 over Okada and Maturi. The same applies to Claims 43 - 47 because they all depend (directly or indirectly) from Claim 42, to Claim 60 because it depends from Claim 59, to Claims 69 - 73 because they all depend (directly or indirectly) from Claim 68, and to Claim 80 because it depends from Claim 79.

New dependent structure Claim 83 recites that the decoder system further includes "a memory management unit (a) for controlling transfer of the encoded video data to and from the video input buffer and (b) for controlling transfer of the encoded audio data to and from the audio input buffer". New dependent method Claim 85 similarly recites that "a memory management unit" is utilized "to control transfer of the encoded video data to and from the video input buffer" and "to control transfer of the encoded audio data to and from the audio input buffer".

Neither Okada nor Maturi discloses a memory management unit, let alone a memory management unit for controlling transfer of encoded audio and video data as required by each of Claims 83 and 85. Accordingly, Claims 83 and 85 are separately patentable over Okada and Maturi. Claims 84 and 86 respectively depend from Claims 83 and 85 and are therefore also separately patentable over Okada and Maturi.

Claims 53, 54, 76, and 77 have once again been rejected under 35 USC 103(a) as obvious based on Okada and Maturi in view of Nuber et al. ("Nuber"), U.S. Patent 5,703,877. Claim 61 has once again been rejected under 35 USC 103(a) as obvious based on Okada and Maturi in view of Terashima et al. ("Terashima"), U.S. Patent 6,163,647. These rejections are respectfully traversed.

Claims 53, 54, and 61 each depend (directly or indirectly) from Claim 41 rejected as obvious based on Okada and Maturi. Claims 76 and 77 each depend (directly or indirectly) from Claim 67 likewise rejected as obvious based on Okada and Maturi. For the reasons presented above, neither of Claims 41 and 67 is obvious based on Okada and Maturi. Nothing in Nuber or/and Terashima would justify combining Okada and Maturi so as to

make Claim 41 or 67 obvious. Consequently, Claims 53, 54, 61, 76, and 77 are variously patentable over Okada, Maturi, and Nuber or Terashima for the same reasons that Claims 41 and 67 are patentable over Okada and Maturi.

In summary, the 35 USC 132 new-matter objection to the specification should be withdrawn. Claims 41 - 86 have been shown to be patentable over the applied art. Consequently, Claims 41 - 86 should be allowed so that the application may proceed to issue.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

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